REMARKS

After entering of the proposed amendments set forth above, claims 1-30 remain in this application. Claims 1, 3, 4, 6, 9, 11, 12, 17, 19, 20, 25, and 30 have been amended. No new matter has been added. Applicant respectfully requests that the above-identified application be reconsidered in view of the following remarks.

The Examiner will first note that claims 6 and 9 have been amended herein to correct typographical errors. Claim 6 is corrected such that --in-- was replaced with --is--. Claim 9 is corrected such that --A-- is replaced with --An--.

The 35 U.S.C. § 112 Rejection

Claims 4, 12, and 20 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which is regarded as the invention. The examiner asserts that the language "the other line" has an insufficient antecedent basis. The amended claims correct any indefiniteness that may have existed. Claims 3, 11, and 19 have been amended such that "another line" is changed to "an other line," which definitively expresses the line referenced because the language is consistent with the language "other line," used in claims 4, 12, and 20. Further, definitiveness is improved through the use of "said other line" in claims 4, 12, and 20. Reading "an other line" from claims 3, 11, and 19, with claim 4, 12, and 20's "said other line" corrects any issues concerning the distinctness of the claim language. Accordingly, reconsideration and withdrawal of the rejections of claims 4, 12, and 20 under 35 U.S.C. § 112, second paragraph is respectfully requested.

The 35 U.S.C. § 102 Rejection

Claims 1-5, 9-13, 17-21, and 25-30 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,802,568 to Csoppenszky ("Csoppenszky"). Claims 1, 9, 17, 25, and 30 have been amended. For example, claim 1 has been amended to include the additional limitation:

...indicating that a line storing valid data in the cache is a candidate for replacement by reducing the importance level of the line. (Emphasis added).

In view of the amendments and remarks, reconsideration and withdrawal of the rejection of claims 1-5, 9-13, 17-21, and 25-30 and claims 6-8, 14-16, and 22-24 which depend from claims 1, 9, and 17, respectively, is respectfully requested.

The Present Invention

An embodiment of the present invention pertains to a method for reducing an importance level of a cache line. In a cache system there may exist many entries, or "lines." Because cache memory is expensive, cache memory is limited in size. Therefore, different replacement policies have been devised to determine which line of cache is to be replaced when the cache is full with valid data. A goal common to all replacement policies is to reduce the amount of cache "misses" that may occur in future attempts to retrieve valid data from the cache. Cache misses occur when a valid copy of data is not available in a cache memory. In the present invention, as amended, cache misses are reduced through an instruction to the cache that reduces the importance of a cache line storing valid data. By reducing the importance of a cache line, the cache line is a candidate for replacement, for example, because that cache line "will not be used as soon as other data." (page 7, line 8).

According to an embodiment of the present invention, cache lines are not invalidated because a cache line is merely indicated as a candidate for replacement. An example of an embodiment of the present invention presented in the specification and

drawings shows that a cache line storing valid data is still valid after it is indicated as a candidate for replacement. In Figure 3, between columns 36-37, an embodiment of the present invention lowers the importance of b, located in 1. At that time, in column 38, b still exists in cache entry 1 and is valid. It is valid because, as one could see from earlier memory accesses, memory which is least important is still valid. An example of a memory access of least important data is depicted in Figure 3, columns 35-36. In column 35, b is a candidate for replacement. In the following memory access, there is a call for b in column 36. At this time, there is a cache hit because in column 36 of Figure 3, b had not been replaced. Thus, lowering the importance of a cache line, like b, retains the validity of the data in that cache line.

The Csoppenszky Reference

Csoppenszky includes a reference to the possibility of translation look-aside buffer ("TLB") entries being invalidated by a "processor core." The TLB is a type of cache that may be used in a computer system. The examiner has elaborated on the reference and asserts that cache entries can be invalidated by the processor core, for a number of reasons. The examiner admits that the Csoppenszky reference does not allow for a cache line to be valid after it is selected by the processor core, rather it invalidates the lines entirely. The Csoppenszky reference refers to a method of retaining the most recently used entry in a cache.

Argument

The reference in the Csoppenszky reference fails to teach or describe reducing an importance level of a cache line storing valid data. The proper standards for use in anticipation rejections according to MPEP can be found in section 2131. Section 2131 quotes the standard from Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987), "a claim is anticipated only if each and

every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference."

The examiner rejected claims 1, 9, 17, 25, 26, and 30 asserting that they are anticipated by a reference within Csoppenszky. The reference asserted by the examiner indicates that a processor can invalidate a line of cache. The examiner uses the reference to assert that invalidation can happen for a number of reasons. In contrast, the rejected claims recite a lowering of the importance of a cache line, leaving it valid. The newly amended claims, specification, and drawing present that a cache line is still valid after it has been reduced in importance according to an embodiment of the present invention. Because the lowering of importance of cache line is different from invalidating a cache line, Czoppenszky does not anticipate these claims. Accordingly reconsideration of the rejection of these and claims 2-8, 10-16, 18-24, and 27-29 which ultimately depend from claims 1, 9, 17, 25, and 26, respectively under 35 U.S.C. § 102(b), is respectfully requested.

As to the rejection of claims 2, 9, 10, 18, 27, and 30, the examiner asserts that by invalidating a cache line, the cache line's importance is reduced. As argued above, reducing the importance of a cache line in the presently claimed invention leaves a cache line valid. Accordingly, reconsideration of the rejection of these claims and claims 3-4, 11-16, 19-20, and 28 which depend from claims 2, 9-10, 18, and 27 respectively under 35 U.S.C. § 102(b), second paragraph, is respectfully requested.

The 35 U.S.C. § 103 Rejection

Claims 6, 7, 14, 15, 22, and 23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Csoppenszky and U.S. Patent No. 6,314,561 to Funk et al. ("Funk").

In the Office Action, it is conceded that Funk does not cover the reduction of the importance of a cache line. Thus, Funk fails to make up for the deficiencies of

Csoppenszky. Accordingly, reconsideration of the rejection of these claims under 35 U.S.C. § 103(a), is respectfully requested.

Claims 8, 16, and 24 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Csoppenszky and U.S. Patent No. 4,713,755 to Worley ("Worley").

The Present Invention in Dependent Claims 8, 16, and 24

Dependent claims 8, 16, and 24 includes the embodiment of the present invention as an extension of a memory access instruction. This element is elaborated upon in the specification, wherein the claimed invention is differentiated as an independent instruction or an extension of a memory access instruction. As an independent memory access instruction, the present invention may be embodied as an instruction by itself, for example, RICL(b). (page 4, lines 23-26). In contrast, as an extension of a memory access instruction, the present invention would be part of another instruction that accesses memory. The specification gives the example of a store instruction, which would include an instruction to reduce the importance of a line in a cache.

Worley

Worley describes a system where a cache is managed through instructions that flush cache lines. The instructions in the specification of Worley are all independent instructions, and none of these instructions are used with another memory access instruction. (col. 4, lines 31-35). The examiner asserts that Worley covers instructions that are an extension of a memory access instruction, but it is unclear from Worley how that would be done.

Argument

The examiner asserts that Worley covers an instruction that is an extension of a memory access instruction. The applicant respectfully disagrees. The language "an

extension of a memory access instruction," refers to an instruction of the current invention being related to an other instruction that accesses memory, for example, a store instruction. The specification of the present invention describes this embodiment clearly and gives an example. (page 4, lines 23-26). The examiner does not address whether this subject matter is covered by Worley, and it is not, nor can it be found implicitly in Worley. (col. 4, lines 31-35).

Also, since Worley does not teach or suggest reducing the importance of a cache line of valid data, Worley fails to make up for the deficiencies of Csoppenszky. Accordingly, reconsideration of the rejection of these claims under 35 U.S.C. § 103(a), is respectfully requested.

CONCLUSION

For all the above reasons, the Applicant respectfully submit that this application is now in condition for allowance. A Notice of Allowance is earnestly solicited.

The Examiner is invited to contact the undersigned at (408) 975-7500 to discuss any matter concerning this application. The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. § 1.16 or § 1.17 to Deposit Account No. 11-0600.

Respectfully submitted,
KENYON & KENYON

Dated: 8/1/02

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Version with Markings to Show Changes Made

IN THE CLAIMS:

Marked up versions of amended claims 1, 3, 4, 6, 9, 11, 12, 17, 19, 20, 25, and 30 follow:

1. (Amended) A method for [reducing an importance level of a line in a memory of a cache, the method comprising] controlling a cache, comprising:

providing an instruction to the cache indicating that [the] a line storing valid data in the cache is a candidate for replacement by reducing an importance level of the line.

3. (Amended) The method as recited in claim 2 wherein the reducing of the importance level of the line results in the line being replaced prior to [another] an other line scheduled for replacement by a replacement policy of the cache.

4. (Amended) The method as recited in claim 3 wherein the replacement policy is a least recently used policy and wherein [the] said other line is less recently used than the line.

6. (Amended) The method as recited in claim 1 wherein the instruction [in] is part of an application kernel.

9. (Amended) [A] An instruction for increasing hit rate of a cache, the instruction comprising an indication that a line storing valid data in a memory of the cache is a candidate for replacement by reducing an importance level of the line.

11. (Amended) The instruction as recited in claim 10 wherein the reducing of the importance level of the line results in the line being replaced prior to [another] an other line scheduled for replacement by a replacement policy of the cache.

12. (Amended) The instruction as recited in claim 11 wherein the replacement policy is a least recently used policy and wherein [the] said other line is less recently used than the line.

17. (Amended) An article comprising a storage medium, the storage medium having a set of instructions, the set of instructions being capable of being executed by at least one processor to implement a method for [reducing an importance level of a line in a memory of a cache] controlling a cache, the set of instructions when executed comprising providing an indication to the cache that [the] a line storing valid data in the cache is a candidate for replacement by reducing an importance level of the line.

19. (Amended) The article as recited in claim 18 wherein the reducing of the importance level of the line results in the line being replaced prior to [another] an other line scheduled for replacement by a replacement policy of the cache.

20. (Amended) The article as recited in claim 19 wherein the replacement policy is a least recently used policy and wherein [the] said other line is less recently used than the line.

25. (Amended) A cache comprising:

a cache memory including a cache line storing valid data; and

a cache control logic for reducing an importance level of the cache line based on an instruction.

30. (Amended) A method for [reducing an importance level of a line in a memory of a cache] controlling a cache, comprising:

providing an instruction to the cache indicating that [the] a line storing valid data is a candidate for replacement by reducing an importance level of the line; and

reducing an importance level of the line based on the instruction.